Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 2, 3, 10, 17, 23, 24, 28-32, 35, 43, and 49, and amend claims 1, 9, 16, 22, 33, 38, and 45, as follows:

Listing of Claims:

1. (Currently Amended) A computer system, comprising:

a central processing unit (CPU);

~~a first bus~~ a local CPU bus coupled to the CPU;

a memory coupled to the ~~first~~ local CPU bus to store data accessible by the CPU via the ~~first~~ local CPU bus;

~~a second bus~~ a PCI bus coupled to the ~~first~~ local CPU bus to provide communication with the CPU and the memory via the local CPU bus; ~~and~~

a PC card coupled to the ~~second~~ PCI bus, the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system; and

a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and the PC card coupled to the PCI-CardBus bridge.

2-3. (Cancelled)

4. (Original) The computer system of claim 1 wherein the non-volatile memory of the PC card comprises a flash memory device.

5. (Previously Presented) The computer system of claim 1 wherein the PC card further includes a bus interface coupled to the PCI bus, and further coupled to the non-volatile memory and the controller to transfer data between the non volatile memory and the PCI bus in accordance with a data format and transfer protocol of the PCI bus.

6. (Original) The computer system of claim 1, further comprising a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information.

7. (Original) The computer system of claim 1, further comprising compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively.

8. (Original) The computer system of claim 1 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

9. (Currently Amended) A computer system, comprising:

a central processing unit (CPU);

a memory coupled to the CPU to store data accessible by the CPU;

a bus coupled to the CPU and memory to provide communication therewith; ~~and~~

a PC card coupled to the bus, the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system; and

wherein the bus comprises a PCI bus, and the computer system further comprises a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and the PC card coupled to the PCI-CardBus bridge.

10. (Cancelled)

11. (Original) The computer system of claim 9 wherein the non-volatile memory of the PC card comprises a flash memory device.

12. (Previously Presented) The computer system of claim 9 wherein the PC card further includes a bus interface coupled to the bus, and further coupled to the non-volatile memory and the controller to transfer data between the non volatile memory and the bus in accordance with a data format and transfer protocol of the bus.

13. (Original) The computer system of claim 9, further comprising a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information.

14. (Original) The computer system of claim 9, further comprising compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively.

15. (Original) The computer system of claim 9 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

16. (Currently Amended) An apparatus for capturing and restoring a machine state of a computer system having a central processing unit (CPU) coupled to a memory via a first bus, and further having a ~~second~~ PCI bus coupled to the first bus to provide communication with the CPU and the memory, the apparatus comprising:

a PC card coupled to the ~~second~~ PCI bus, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; ~~and~~

a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system; and

a bus interface compatible with a CardBus and coupled to the PCI bus, the bus interface further coupled to the non-volatile memory and the controller to transfer data between the non volatile memory and the PCI bus in accordance with a data format and transfer protocol of the PCI bus.

17-18. (Cancelled)

19. (Original) The apparatus of claim 16 wherein the non-volatile memory comprises a flash memory.

20. (Original) The apparatus of claim 16 wherein the transfer component comprises:

a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory; and

a download component for directing the controller to transfer data from the non-volatile memory to the CPU and the memory.

21. (Original) The apparatus of claim 16, further comprising compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively.

22. (Currently Amended) An apparatus for capturing and restoring a machine state of a computer system having a central processing unit (CPU) coupled to a memory, and further having a PCI bus coupled to the CPU and memory to provide communication with the CPU and the memory, the apparatus comprising:

a PC card coupled to the PCI bus, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; ~~and~~

a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state

information for capturing and restoring, respectively, a corresponding machine state of a computer system; and

a CardBus compatible bus interface coupled to the PCI bus, and further coupled to the non-volatile memory and the controller to transfer data between the non volatile memory and the PCI bus in accordance with a data format and transfer protocol of the PCI bus.

23-24. (Cancelled)

25. (Original) The apparatus of claim 23 wherein the non-volatile memory comprises a flash memory.

26. (Original) The apparatus of claim 23 wherein the transfer component comprises:

a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory; and

a download component for directing the controller to transfer data from the non-volatile memory to the CPU and the memory.

27. (Original) The apparatus of claim 23, further comprising compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively.

28-32. (Cancelled)

33. (Currently Amended) A computer system, comprising:

a central processing unit (CPU);

a local CPU bus coupled to the CPU;

a memory coupled the local CPU bus to store data accessible by the CPU via the local CPU bus;

a PCI bus coupled to the local CPU bus to provide communication with the CPU and the memory via the local CPU bus;

a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device;

a CardBus compatible PC card coupled to PCI-CardBus bridge, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; ~~and~~

a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system; and

wherein the PC card further includes a bus interface coupled to the PCI bus, and further coupled to the non-volatile memory and the controller to transfer data between the memory and the PCI bus in accordance with the PCI data format and transfer protocol.

34. (Original) The computer system of claim 33 wherein the non-volatile memory of the PC card comprises a flash memory device.

35. (Cancelled)

36. (Original) The computer system of claim 33, further comprising compression and decompression components for compressing the machine state information to be stored in the non-volatile memory and decompressing the stored compressed machine state information to be downloaded, respectively.

37. (Original) The computer system of claim 33 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

38. (Currently Amended) In a computer system having a central processing unit (CPU) coupled to a memory, and further having a bus coupled to the CPU and memory to

provide communication therewith, a method for storing a machine state of the computer system, comprising:

capturing the machine state of the computer system via a controller coupled to a non-volatile memory to control the storing of data therein and the retrieval of data therefrom;

transferring machine state information corresponding to the captured machine state from the computer system to a PC card operably configured with the non-volatile memory; ~~and~~

storing the machine state information in the non-volatile memory in order to restore the stored machine state when the machine state information is provided to a computer system; and

wherein transferring the machine state information to the PC card comprises transferring data from the CPU and the memory to the PC card in accordance with a CardBus protocol.

39. (Original) The method of claim 38 wherein capturing, transferring and storing the machine state information is in response to executing a power down procedure.

40. (Original) The method of claim 38 wherein capturing, transferring and storing the machine state information is in response to a user request.

41. (Original) The method of claim 38 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

42. (Original) The method of claim 38 wherein capturing the machine state of the computer system comprises:

capturing data present in the memory; and

capturing data present in registers of the CPU.

43. (Cancelled)

44. (Original) The method of claim 38, further comprising compressing the machine state information to be stored in the non-volatile memory.

45. (Currently Amended) A method for restoring a machine state to a computer system having a central processing unit (CPU) coupled to a memory, and further having a bus coupled to the CPU and memory to provide communication therewith, the method comprising:

identifying machine state information corresponding to the machine state to which the computer system is to be restored stored in a non-volatile memory included in a PC card;

transferring the machine state information from the non-volatile memory to the computer system via a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; ~~and~~

writing data of the machine state information to the memory and CPU in order to restore the computer system to the identified machine state; and

wherein transferring the machine state information from the non-volatile memory comprises transferring data from PC card to the computer system in accordance with a CardBus protocol.

46. (Original) The method of claim 45 wherein identifying, transferring and writing the machine state information is in response to executing a power up procedure.

47. (Original) The method of claim 45 wherein identifying, transferring and writing the machine state information is in response to user request.

48. (Original) The method of claim 45 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

49. (Cancelled)

50. (Original) The method of claim 45 wherein the machine state information stored in the non-volatile memory is in a compressed data format, and the method further comprises decompressing the machine state information to be transferred to the computer system.